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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,452	06/23/2003	Kenji Kohno	4041P-20/DVA	9754

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EXAMINER	
KITOV, ZEEV	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	10/601,452	KOHNO, KENJI	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 13, 16 - 24, 27 - 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29 - 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1 - 13, 16 - 24, 27, 28, 36 - 39* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Pri rity under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges reception of the Applicant's Response to Election of Species. The Applicant selected the Species 15 Embodiment illustrated in Fig. 27. According to him, the Claims 29 – 32 and 35 read on the elected species. However, during examination Examiner found the Claims 33 and 34 as fitting the Species 15 area. The examination was conducted accordingly covering Claims 29 - 35.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rodriguez et al. (US 5,815,356) in view of Rogers (US 5,049,763). Rodriguez et al. disclose most of the elements of Claim 29 including a semiconductor device having an insulated gate transistor (element Q3 in Fig. 2) disposed in a current path of an electric load; a gate voltage boosting element (elements Q1, Q2, Z1, Z2, and charge pump, element 4, in Fig.2, col. 7, lines 37 - 63) having one end connected to a gate electrode of said insulated gate transistor so as to operate in response to a surge applied from a high-voltage terminal of said insulated gate transistor. However, it does not disclose a wiring member having a parasitic inductance. Rogers discloses a wiring member

serving as a parasitic inductance (elements L in Fig. 1). In the Rodriguez et al. system modified according to Rogers, the wiring member of the reference is being connected in parallel with the gate voltage - boosting element with respect to the high-voltage terminal of the insulated gate transistor. Both references have the same problem solving area, namely providing switching IC circuits immune to the power rail disturbances. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Rodriguez et al. solution by adding the inductive anti-bounce circuit of Rogers, because as Rogers states (col. 2, lines 9 – 23), it provides anti-bounce protection to the circuit.

As to the transistor and the gate voltage-boosting element being formed in a chip, according to Rodriguez et al. (col. 7, lines 30 – 35), the whole circuit can be fabricated in a conventional TO-220 package, which is a power integrated circuit. Leaving the inductor element outside the chip is a routine designer decision based on his secondary considerations.

Regarding Claim 33, Rodriguez et al. disclose the gate voltage-boosting element including a zener diode (elements Z1 and Z2 in Fig. 2).

Regarding Claim 34, Rodriguez et al. disclose the gate voltage-boosting element as a combination of plurality of circuit elements including the zener diode (elements Z1 and Z2 in Fig. 2) and bipolar transistor (elements Q1 and Q2 in Fig. 2).

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rodriguez et al. in view of Rogers and Chrysostomides et al. (US 5,646,434). As was

stated above, Rodriguez et al. and Rogers disclose all the elements of Claim 29. However, regarding Claim 30, they do not disclose a wiring member as a bonding wire. Chrysostomides et al. disclose the wiring members as the bonding wires (elements 6 – 9 in Fig. 5). Both references have the same problem solving area, namely providing the esd protection for semiconductor devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Rodriguez et al. solution by adding the bonding wire as the wiring member according to Crysostomides et al., because (i) as Crysostomides et al. state (col. 4, line 59 – col. 5, line 4), the bonding wires have an inductive effect and (ii) use of the bonding wires for connection between the chip and the leads is a method of connection universally used in the semiconductor industry.

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rodriguez et al. in view of Rogers, Mekdhanasarn et al. (US 5,796,570) and Lin et al. (US 5,818,086). As was stated above, Rodriguez et al. and Rogers disclose all the elements of Claim 29. However, regarding Claim 31, they do not disclose a resin molded chip and a specific structure of the wiring member. Mekdhanasarn et al. disclose the wiring member having a bonding wire (elements 24 in Fig. 2) and a lead frame (element 42 in Fig. 2) and PCB (element 38 in Fig. 2). As to a conductive pattern formed on the PCB, the printed conductive pattern is an inherent feature of the PCB. Both references have the same problem solving area, namely providing ESD protection for the semiconductor elements. Therefore, it would have been obvious to one of

ordinary skill in the art at the time the invention was made to have further modified the Rodriguez et al. solution by encapsulating the die according to Mekdhanasarn et al., since it is well known in the art that the bonding wires are universally used elements of interconnection between the die and the leads of the IC circuit and that the lead frame is necessary for carrying these leads. If further discloses the embedded chip, however without explicitly disclosing the embedding material.

Lin et al. disclose the resin embedded chip (col. 1, lines 34 – 37). Both references have the same problem solving area, namely providing ESD protection for the semiconductor devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Rodriguez et al. solution by using the resin as a material for embedding the chip according to Lin et al., because it is a common material for chip embedding in the electronic devices manufacturing having advantages of a low manufacturing cost and high reliability.

Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rodriguez et al. in view of Rogers and Costa et al. (US 5,578,860). As was stated above, Rodriguez et al. and Rogers disclose all the elements of Claim 29. However, regarding Claim 32 they do not disclose a conductive pattern formed on the semiconductor substrate. Costa et al. disclose a wiring member (shown in Fig. 4) as a conductive pattern formed on the semiconductor substrate (col. 5, lines 29 – 45). Both references have the same problem solving area, namely providing ESD protection to the semiconductor devices. Therefore, it would have been obvious to one of ordinary

skill in the art at the time the invention was made to have further modified the Rodriguez et al. solution by using the wiring member in form of conductive pattern formed on the semiconductor substrate according to Costa et al., because as well known in the art, such method of forming the wiring element has number of advantages, including high reliability.

As to the limitation of mounting chip on a semiconductor substrate by using the flip chip bonding method, it is the product-by-process limitation and is treated in accordance with MPEP 2113 rule.

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rodriguez et al. in view of Rogers and Williams (US 5,517,379). As was stated above, Rodriguez et al. and Rogers disclose all the elements of Claim 29. However, regarding Claim 35 they do not disclose a particular circuit implementation of the gate voltage-boosting element. Williams discloses the gate voltage-boosting element as a combination of plurality of capacitors (elements C1 – C3 and diodes D4, D5, D7 – D9 in Fig. 3). Both references have the same problem solving area, namely providing a voltage protection to the semiconductor devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Rodriguez et al. solution by adding the voltage boosting element of Williams, because the Williams solution, the voltage multiplier circuit is a common in the art solution, which is taught in college courses of Analog Electronics.

C nclusi n

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.
07/09/2004

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